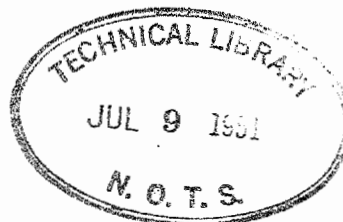


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THE DESIGN AND CONSTRUCTION OF A D-C AMPLIFIER  
FOR USE WITH THE AVIATION ORDNANCE DEPARTMENT  
ANALOG COMPUTER

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U. S. NAVAL ORDNANCE TEST STATION  
China Lake, California

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FOREWORD

The Naval Ordnance Test Station does not wish to claim credit for the development of the basic circuits of the amplifier described in this report. Acknowledgement is made of the similarity of this amplifier to analog computer amplifiers manufactured and in use by the Bell Telephone Laboratories, Radio Corporation of America, and Reeves Instrument Company. The particular design of the amplifier described in this report was chosen to supplement the present analog computer equipment now being used by the Aviation Ordnance Department

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ABSTRACT

This report presents details of a d-c amplifier which was designed for use as a feedback amplifier with an analog computer.

It is shown that with the proper series and feedback components the amplifier may be used for summing, multiplying, differentiating, integrating, and combined operations. Multiplication by quantities up to 1000 is expected to be possible, outputs of up to  $\pm 100$  volts at 10 ma are available, and accuracy is good.

The operation of a chopper circuit which keeps the input grid at ground potential is described. Other circuit operations are described, and circuit diagrams for both the amplifier and its power supply are included.

Amplifier and power supply construction is discussed, and layout diagrams are included.

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### INTRODUCTION

The d-c amplifier described here has been designed for use with the Aviation Ordnance Department analog computer. The operation of this computer is described in Technical Memorandum 4529-23 entitled "NOTS Analog Computing Facility," by V. R. Briggs.

This report describes the amplifier, discusses its operation, and evaluates its performance when used as a multiplier, an integrator, or a differentiator. The amplifier maintains its output grid very nearly at ground potential by use of a chopper circuit. The feedback amplification for the frequencies of interest is very high, the stability is good, and the output impedance is sufficiently low for most purposes.

The circuit diagram of a single amplifier is shown in Dwg. SK 331323 while a layout diagram for a bank of ten amplifiers is shown in Dwg. SK 332324. The group of ten amplifiers is supplied from a single power supply whose circuit and layout are shown in Dwg. SK 331325 and Dwg. SK 331326, respectively. These circuits are discussed in the following pages.

### GENERAL DESCRIPTION

The circuit of the amplifier is shown in Dwg. SK 331323. In this drawing no series input or feedback elements are shown, but they must be considered in evaluating the circuit performance. In actual use these external components are connected between terminals on a breadboard which is external to the amplifier cabinet. Connections between these external terminals and the amplifiers are made through shielded leads. Figure 1 (a, b, and c) illustrates the use of the amplifier as an integrator, summer and multiplier, or differentiator by use of the proper series and feedback components. A generalized circuit is shown in Fig. 1 (d) in which both input and feedback impedances use parallel resistor-condenser combinations. The circuits of Fig. 1 (a, b, and c) may be derived from this circuit, and other circuits may be derived by using single series or feedback elements in combination with parallel elements in the other impedance. The general circuit may be used to perform several operations in one amplifier. In particular, it might be used to set up network transfer functions so that the response of a circuit to its input might be found using only a few amplifiers.

### PRELIMINARY DATA

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One of the most important functions of the amplifier circuitry is to maintain the grid of the input tube (V1) at ground potential. In operation, any deviation of this grid from ground results in an a-c signal at the grid of V2, through the action of the chopper in grounding the d-c signal at a 60 cycle/sec rate. This a-c signal is approximately a square wave whose peak to peak amplitude is equal to the difference in voltage between the grid of V1 and ground. This square wave is amplified in two stages and then synchronously rectified by the chopper which acts in the manner of a clamp circuit. The rectified wave is then filtered through a Pi section RC filter which attenuates frequencies above three to five cycles, and thus eliminates the 60 cycle components of the rectified wave. The resulting signal is cathode coupled through the other half of V1, then amplified through the rest of the amplifier, and fed back through the feedback element to the grid of V1 where it is of such polarity as to correct the deviation of the grid from ground potential. The gain of the chopper section of the amplifier is about 120, and the gain through the rest of the amplifier is about 16,000 so the effective gain of the amplifier for frequencies from d-c up to about 3 cycles is nearly 2,000,000.

Measurements showed that the input grid might be adjusted to within several hundred microvolts of ground potential with relative ease. When the input grid is zeroed as well as possible with a filament supply voltage of about 6.4 volts, it is found that the grid voltage varies between about -1.7 to 1.7 millivolts when the filament voltage is varied between 5.8 and 7.0 volts. When the amplifier is connected as an integrator, a deviation from ground of 2.0 millivolts at the input grid would cause an error in the output voltage of 0.12 volt at the end of one minute when an RC time constant of 1 is used. Since the time of computer operation is generally no more than 30 seconds, it can be seen that an appreciable variation in filament supply voltage will not cause serious errors in output voltage. When the amplifier is connected as a multiplier or differentiator, an error of 2.0 millivolts in grid zeroing will have a negligible effect on output voltage.

In normal operation the amplifier should be capable of operating with input signals of less than 50 millivolts and with amplifications of more than 1000. The percentage error due to finite amplifier gain made in assuming a multiplication of  $R_2/R_1$  is given by the following expression

$$\text{Error in percent} = \frac{100 R_2}{R_2 + AR_1}$$

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where  $R_1$  = series resistor  
 $R_2$  = feedback resistor  
 $A$  = amplifier gain

Applying this equation it is found that the limit of multiplication for a one per cent error is  $G = 20,000$ . The actual upper limit of multiplication is less than this since there are limitations imposed by the maximum output voltage and the minimum input (voltage necessary to exceed hum voltage and zero deviation voltage). The minimum input voltage will increase as the gain increases since there is then less feedback to eliminate hum and zero deviation. These considerations will probably limit the maximum gain to less than 2000. Integrating periods of more than 1 min. are possible, and accuracy is good under most conditions since a high gain around the feedback loop is provided. The amplifier will supply an output voltage of about 100 rms volts without distortion, and with a 100 volt d-c output the amplifier will operate into a load resistance of 10,000 ohms.

The amplifier has been designed to be stable under all operating conditions. The design involves the use of an attenuating network which is effective in the frequency range of 10,000 to 50,000 cps and lead networks which are effective at high frequencies. In its present form the circuit shows no tendency to oscillate under normal conditions, and remains stable when used as a differentiator with a square wave input.

#### AMPLIFIER CONSTRUCTION

The information necessary for construction of the amplifier and its power supply is given in Drawings SK 331323-6. Insofar as possible components should be mounted on terminal strips and connected to pins on tube socket by short lengths of insulated copper wire. Where it is necessary to have long signal leads, shielded wire should be used in order to minimize stray pickup which might lead to parasitic oscillations. This applies to the cabled leads to the input and output plugs (shown in Dwg. SK 331324) on the front panel and to the leads to the zero test point switch.

The input and output leads from a given amplifier should be connected to corresponding terminals on their respective Jones Plugs. The grid zero switch circuit should be arranged so that the test point jack may be connected to any one of the amplifiers.

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The amplifier chassis is arranged with its tube axes horizontal. This arrangement facilitates tube removal, prevents the trapping of heat under the chassis and permits convection cooling of the tubes.

#### POWER SUPPLY

Amplifier power requirements are such that ten amplifiers may be fed from one power supply of the type shown in the accompanying drawings. This supply provides regulated voltages as follows: (1) 300 volts at 300 ma, (2) 105 volts at 20 ma, (3) -150 volts at 250 ma and (4) -300 volts at 20 ma. Filament transformers supply unregulated 6.3 volts a-c at 25 amperes to the amplifier filaments and choppers.

#### CONCLUSIONS

The operating characteristics of the d-c amplifier described above meet the requirements of the analog computer in which the amplifier will be used. These characteristics are as follows:

- (1) Gain without feedback --- Approximately 2,000,000
- (2) Maximum output current --  $\pm 10$  milliamperes
- (3) Maximum output voltage --  $\pm 100$  volts
- (4) Maximum accurate multiplication -- More than 1000.
- (5) Integration error for  $RC = 1$  -- Less than 0.05 volt/min.

*Melville C. Greusere*

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Aviation Ordnance Department

MCC/hc

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P80 3513

35(2) 3521

3501 3522 (Crockett)

3502 3523

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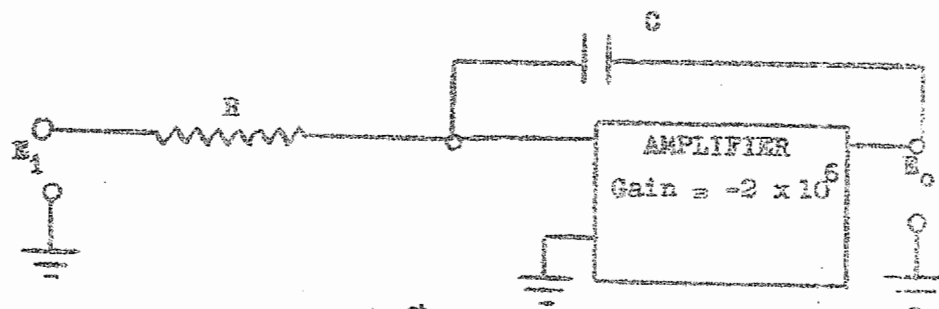
On-Station Distribution approved by

*John H. Gregory*  
J. H. GREGORY, Head  
Development Branch #4

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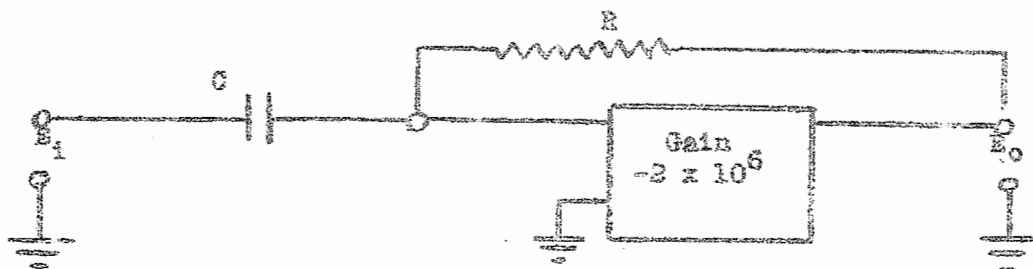
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$$E_o = -\frac{1}{RC} \int E_1 dt$$

$$= -RCp E_1$$

Fig. 1 (a) INTEGRATOR



$$E_o = -RC \frac{dE_1}{dt}$$

$$= -RCp E_1$$

Fig. 1 (b) DIFFERENTIATOR

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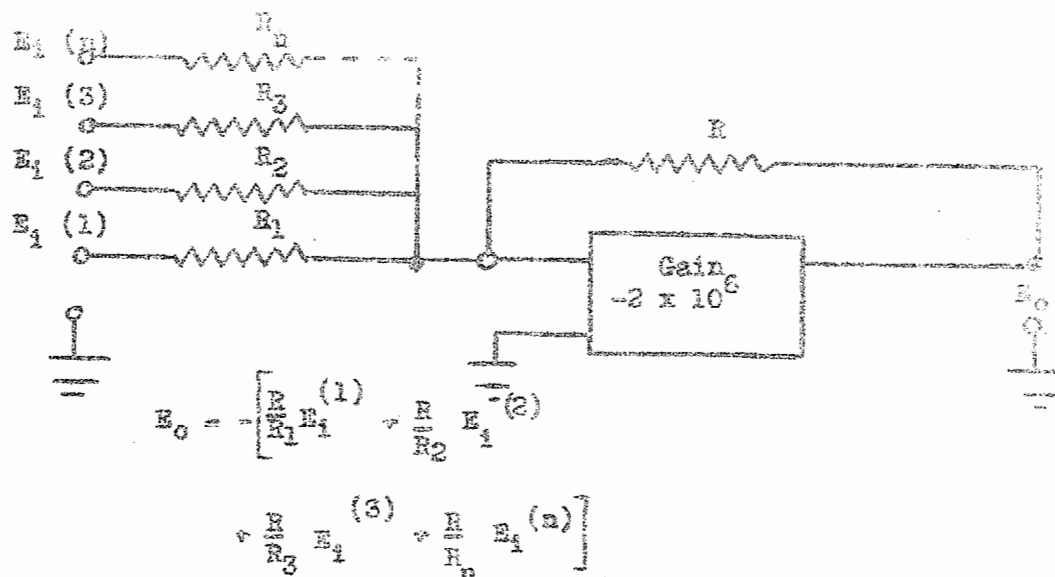
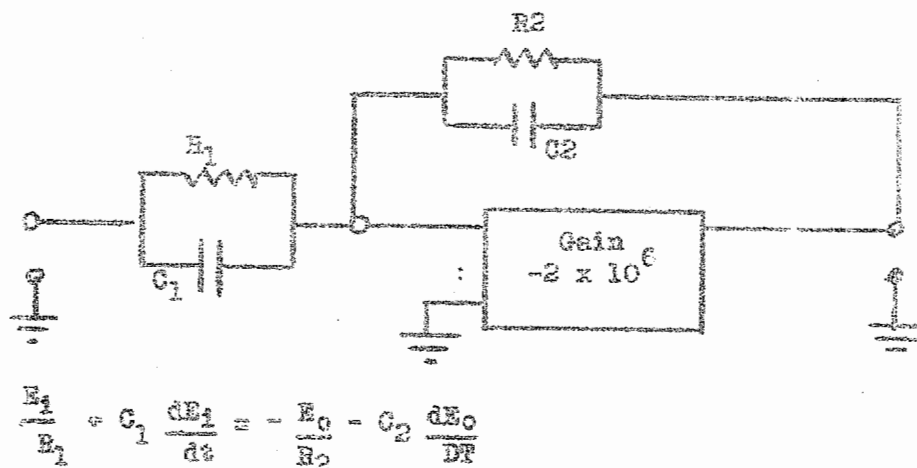


Fig. 1 (c) SUMMER AND MULTIPLIER



OR

$$E_0 = - \frac{R_2}{R_1} \frac{(pC_1R_1 + 1)}{(pC_2R_2 + 1)} E_1$$

$$\text{where } p = \frac{d}{dt}$$

Fig. 1 (d) GENERAL CASE

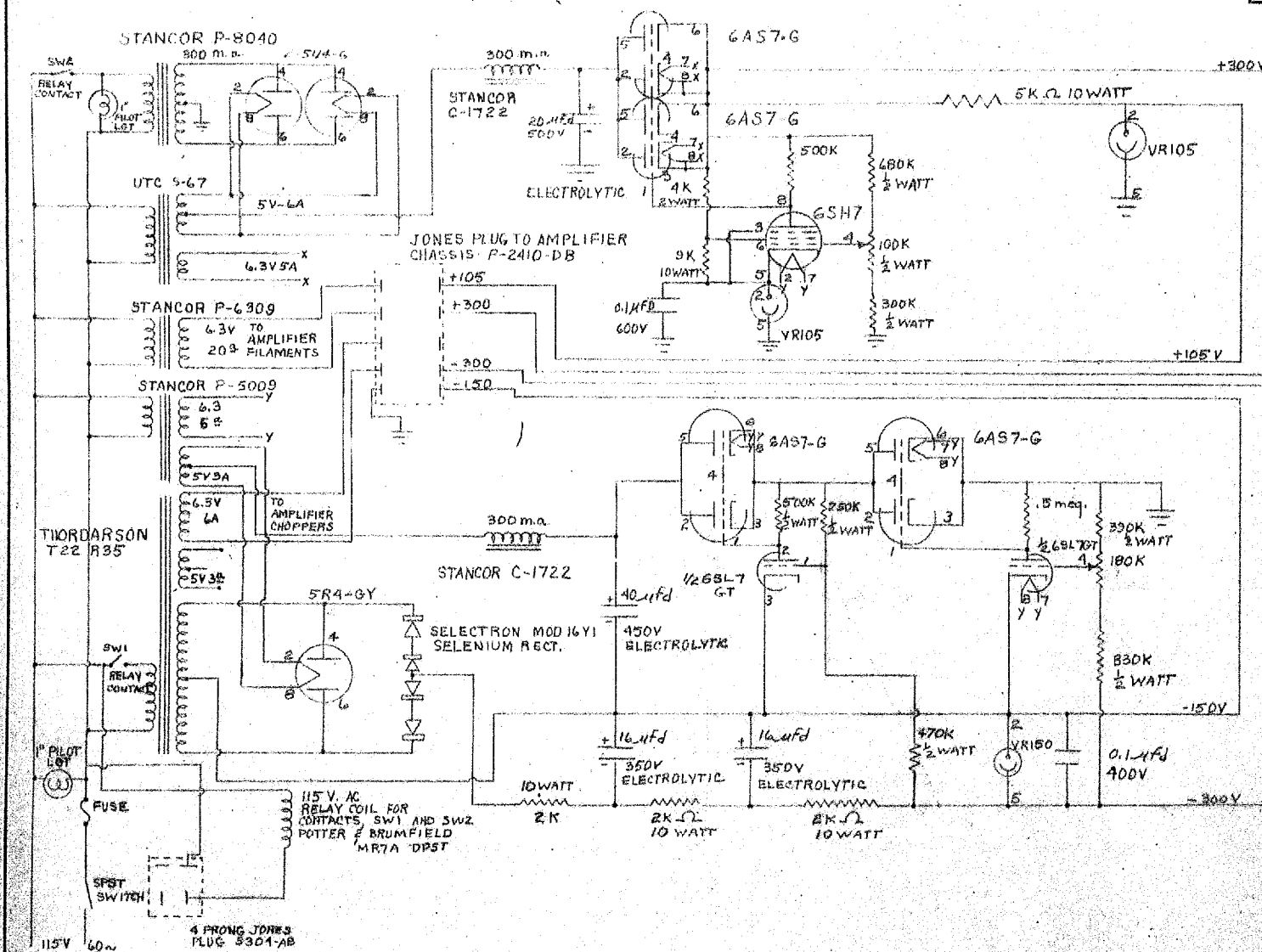
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MATERIAL

DEPT. AUTHENTICATION

APPROVED 10  
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CHECKED 2272 MAY 31/51  
DRAWN 2272 MAY 26/51

POWER SUPPLY  
FOR D.C. AMPLIFIER

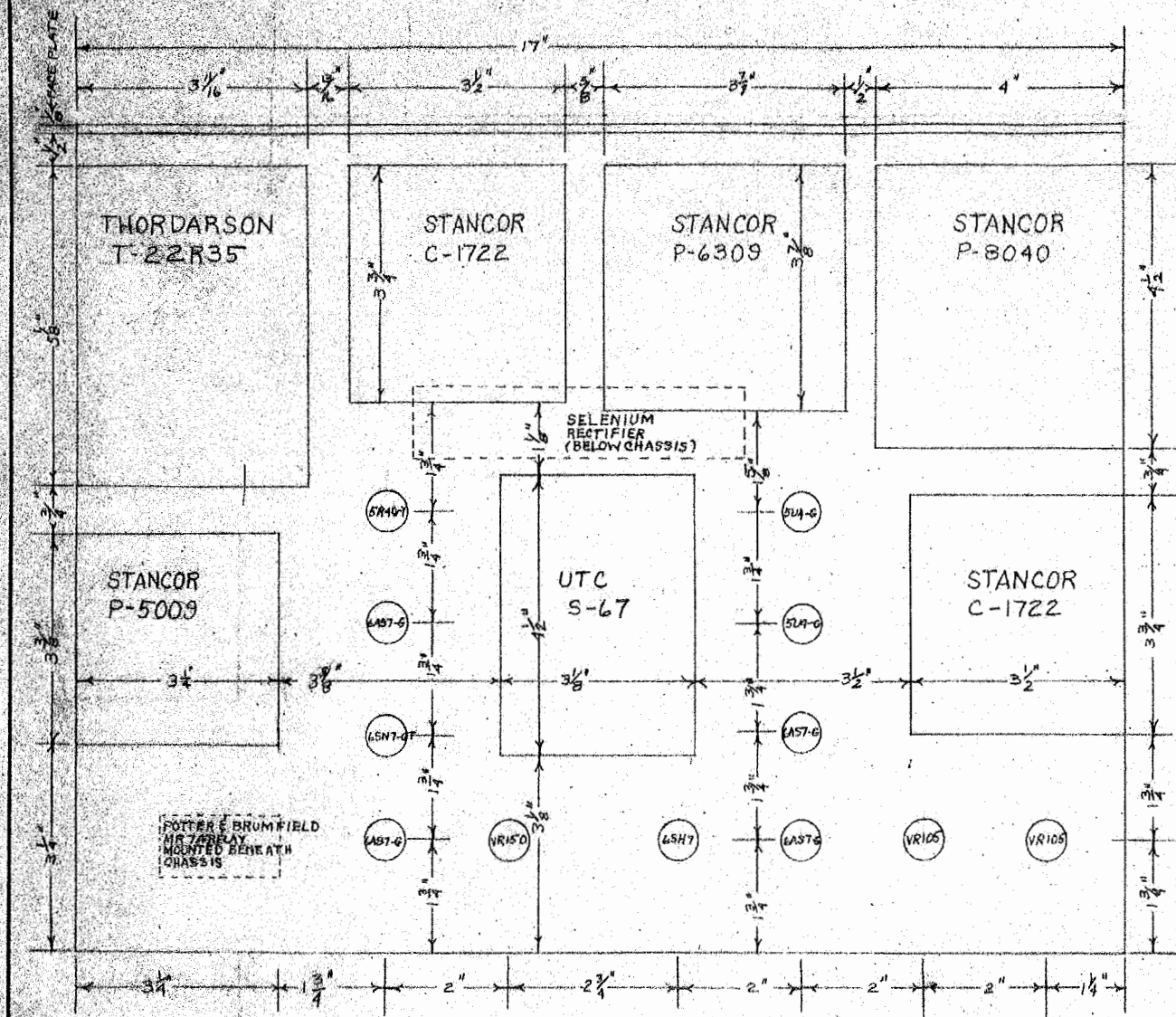
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4 PRONG JONES PLUG (5304-AB),  
SWITCH, PILOT LIGHT FUSE  
HOLDER, AND THREE POTENTIOMETERS  
MOUNTED IN FRONT PANEL.  
TEN PRONG JONES PLUG IS  
MOUNTED ON REAR OF CHASSIS.

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|                                                                                                                      | DRAWN                               | WCB |                                                                   |                                                                                                                                | SK 331326       |